

AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED  
REVISION TO 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

D1 a first circuit configured to generate a second reference signal in response to (i) a first reference signal and (ii) a timing signal, wherein (a) a frequency and a phase of said second reference signal are (i) adjusted in response to said first reference signal and (ii) held when said first reference signal is lost and (b) said first reference signal comprises an external timing signal, wherein said first circuit comprises (i) a digitally controlled reference loop circuit, (ii) a control circuit

5 10 configured to generate a control signal in response to said first and second reference signals, and (iii) said control signal is held when said first reference signal is lost; and

15 a second circuit configured to generate one or more output signals in response to said second reference signal and one of said one or more output signals, wherein said one or more output signals have a controlled and/or substantially zero delay with respect to said first reference signal; and

20 an oscillator configured to generate said second reference signal in response to said control signal and said timing signal.

2. (PREVIOUSLY AMENDED) The apparatus according to  
claim 1, wherein said first circuit comprises:

a control circuit configured to generate a control signal  
in response to said first and second reference signals, wherein  
5 said control signal is held when said first reference signal is  
lost; and

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an oscillator configured to generate said second  
reference signal in response to said control signal and said timing  
signal.

3. (ORIGINAL) The apparatus according to claim 1,  
wherein said second circuit comprises:

a phase locked loop (PLL) circuit configured to generate  
a clock signal in response to said second reference signal and said  
5 one of said one or more output signals; and

a buffer circuit configured to generate said one or more  
output signals in response to said clock signal.

4. (ORIGINAL) The apparatus according to claim 3,  
wherein said second circuit further comprises a divide-by-N circuit  
configured to divide said one of said one or more output signals.

5. (ORIGINAL) The apparatus according to claim 3,  
wherein said PLL circuit comprises an analog PLL circuit.

6. PREVIOUSLY CANCELLED

7. (ORIGINAL) The apparatus according to claim 2,  
wherein said oscillator comprises a voltage controlled crystal  
oscillator (VCXO).

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8. (ORIGINAL) The apparatus according to claim 2,  
wherein said oscillator is an oscillator selected from the group  
consisting of voltage controlled oscillators (VCOs), current  
controlled oscillators (ICOs), digitally controlled oscillators,  
5 digitally controlled crystal oscillators, LC oscillators, RC  
oscillators, and ring oscillators.

9. PREVIOUSLY CANCELLED

10. (ORIGINAL) The apparatus according to claim 5,  
wherein said first circuit further comprises a phase detector  
circuit configured to adjust a phase of said second reference  
signal in response to said first and second reference signals.

11. (ORIGINAL) The apparatus according to claim 1,  
wherein said first circuit further comprises a divide-by-N circuit  
configured to divide a frequency of said first reference signal.

12. (ORIGINAL) The apparatus according to claim 1,  
wherein said apparatus is implemented on a single integrated  
circuit chip.

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13. (PREVIOUSLY AMENDED) An apparatus for generating one  
or more output signals comprising:

means for generating a second reference signal in  
response to (i) a first reference signal and (ii) a timing signal,  
5 wherein (a) a frequency and a phase of said second reference signal  
are (i) adjusted in response to said first reference signal and  
(ii) held when said first reference signal is lost and (b) said  
first reference signal comprises an external timing signal; and

means for generating said one or more output signals in  
10 response to said second reference signal and one of said one or  
more output signals, wherein said one or more output signals have  
controlled and/or substantially zero delay with respect to said  
first reference signal, wherein said apparatus is implemented on a  
single integrated circuit chip.

14. (PREVIOUSLY AMENDED) A method of generating one or more output signals comprising the steps of:

(A) generating a second reference signal in response to

(i) a first reference signal and (ii) a timing signal, wherein (a)

5 a frequency and a phase of said second reference signal are (i) adjusted in response to said first reference signal and (ii) held when said first reference signal is lost and (b) said second reference signal comprises a crystal oscillator signal; and

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(B) generating said one or more output signals in

10 response to said second signal and one of said one or more output signals, wherein said one or more output signals have controlled and/or substantially zero delay with respect to said second reference signal.

15. (ORIGINAL) The method according to claim 14, wherein said second reference signal is phase locked to said first reference signal.

16. (ORIGINAL) The method according to claim 14, wherein step A further comprises the step of dividing said first reference signal by N.

17. (ORIGINAL) The method according to claim 14, wherein step A comprises the step of generating said second

reference signal using a digitally controlled reference loop circuit.

18. (ORIGINAL) The method according to claim 17, wherein step A further comprises the step of adjusting a phase of said second reference signal in response to said first and second reference signals.

19. (ORIGINAL) The method according to claim 14,  
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wherein said first reference signal comprises an external timing signal.

20. PREVIOUSLY CANCELLED

21. (RE-PRESENTED - FORMERLY DEPENDENT CLAIM 3) An apparatus comprising:

a first circuit configured to generate a second reference signal in response to (i) a first reference signal and (ii) a timing signal, wherein (a) a frequency and a phase of said second reference signal are (i) adjusted in response to said first reference signal and (ii) held when said first reference signal is lost and (b) said first reference signal comprises an external timing signal, wherein said first circuit comprises a digitally controlled reference loop circuit; and

a second circuit configured to generate one or more output signals in response to said second reference signal and one of said one or more output signals, wherein (i) said one or more output signals have a controlled and/or substantially zero delay  
15 with respect to said first reference signal and (ii) said second circuit comprises (a) a phase locked loop (PLL) circuit configured to generate a clock signal in response to said second reference signal and said one of said one or more output signals and (b) a buffer circuit configured to generate said one or more output  
20 signals in response to said clock signal.

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